Experiment No. 13

MOSFET AMPLIFIER

AIM:

To obtain the frequency response of MOSFET amplifier in common source configuration with given specifications.

THEORY:

The MOSFET structure has become the most important device structure in the electronics industry. It dominates the integrated circuit technology in Very Large Scale Integrated (VLSI) digital circuits based on n-channel MOSFETs and Complementary n-channel and p-channel MOSFETs (CMOS). The technical importance of the MOSFET results from its low power consumption, simple geometry, and small size, resulting in very high packing densities and compatibility with VLSI manufacturing technology. Two of the most popular configurations of small-signal MOSFET amplifiers are the common source and common drain configurations. The common source circuit is shown below. The common sources, like all MOSFET amplifiers, have the characteristic of high input impedance. High input impedance is desirable to keep the amplifier from loading the signal source. This high input impedance is controlled by the bias resistors R_1 and R_2). Normally the value of the bias resistors is chosen as high as possible. However, too big a value can cause a significant voltage drop due to the gate leakage current. A large voltage drop is undesirable because it can disturb the bias point. For amplifier operation the MOSFET should be biased in the active region of the characteristics.

CIRCUIT DIAGRAM:

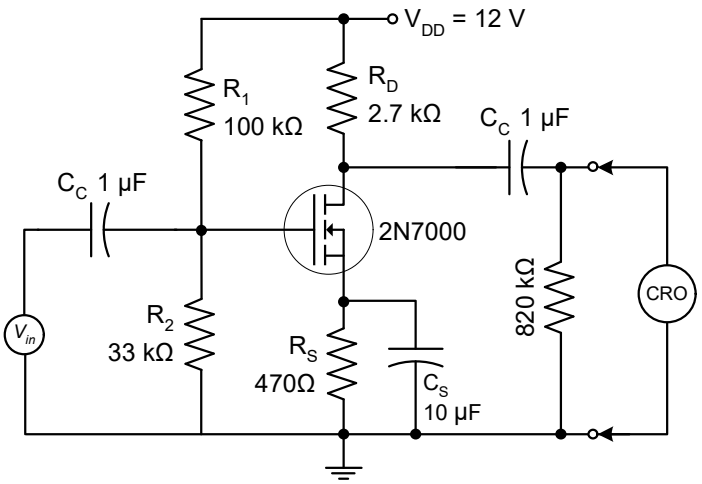

Fig. 1 Circuit diagram of MOSFET amplifier

DESIGN:

Assume V_{DD} = 12V, V_{RD} = 5V, V_{DS} = 6V, I_D = 2 mA

$$R_D = \frac{V_{RD}}{I_D} = \frac{5}{2\times10\times10^{-3}} = 2.5\ \text{k}\Omega$$ use 2.7 kΩ resistor.

Now, the voltage across source side resistance $V_{RS} = V_{DD} - V_{DS} - V_{RD} = 12 - 6 - 5 = 1\,\text{V}$

As, $I_S = I_D$, (no current flows through the gate),

$$R_S = \frac{V_{RS}}{I_D} = \frac{1}{2\times10\times10^{-3}} = 500\ \Omega$$ use 470 Ω resistor.

Voltage – divider bias circuit design:

Assume, R_1 = 100 kΩ. By, voltage division rule, R_2 can be obtained as,

$$V_G = V_{DD} \times \frac{R_2}{R_1 + R_2}$$

Selecting the value of V_G as 4V

$$4 = 12 \times \frac{R_2}{100\times10\times10^3 + R_2} \qquad R_2 \approx 47\ \text{k}\Omega$$

Design of capacitors:

Assume impedance of coupling capacitor be < 1.5 kΩ. Therefore,

$X_{C1} \le 1.5\text{k}\Omega$ ie $\frac{1}{2\pi f C_1} \le 1.5\ \text{k}\Omega$

Given, the frequency of the input signal is 100Hz.

C_1 = 1.06μf. use 1 μf capacitor.

Let $C_1 = C_2$ = 1 μf.

For the bypass capacitor,

$X_{CS} \le 150\Omega$ ie $\frac{1}{2\pi f C_S} \le 150\ \Omega$

C_S = 10μf

PROCEDURE:

Set up the circuit as shown in the figure with an input signal of 0.2V (peak-to-peak) at 1000 Hz. Observe the output on the CRO. Vary the frequency of the input signal over a range of values (from 50Hz to a few MHz) to obtain the frequency response which is a graph between log f (x-axis) and gain in dB (y-axis).

OBSERVATION:

Frequency f Hz	Input voltage V_i V	Output voltage V_i V	Gain $\frac{V_o}{V_i}$ -	Gain $20\log\frac{V_o}{V_i}$ dB

GRAPH (to be obtained):

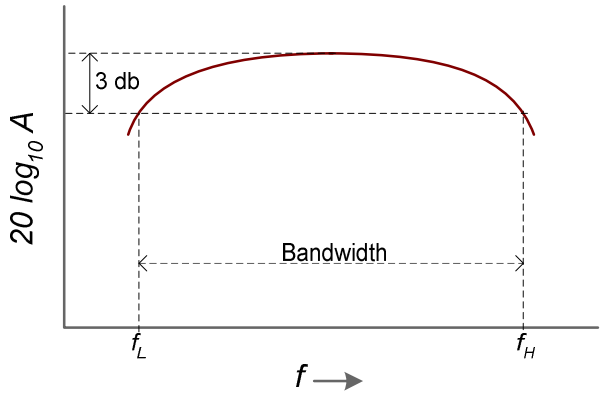

Fig 2. Frequency response

RESULT:

The required common source MOSFET amplifier was designed and set up to obtain the required frequency response.